REMARKS/ARGUMENTS

Claims 1, 2 and 4-20 are pending in the present application. Reconsideration of the claims is respectfully requested. Additionally, a new information disclosure statement is included with this response. Applicants request that the examiner consider the disclosed references and allow the claims.

I. 35 U.S.C. § 102, Anticipation

The Examiner rejected claims 1, 2 and 4-20 under 35 U.S.C. § 102 as anticipated by *Ademmer et al.*, High-Speed Connection Method, U.S. Patent 6,212,643 (April 3, 2001) (hereinafter "*Ademmer*"). This rejection is respectfully traversed.

A prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). All limitations of the claimed invention must be considered when determining patentability. *In re Lowry*, 32 F.3d 1579, 1582, 32 U.S.P.Q.2d 1031, 1034 (Fed. Cir. 1994). Anticipation focuses on whether a claim reads on the product or process a prior art reference discloses, not on what the reference broadly teaches. *Kalman v. Kimberly-Clark Corp.*, 713 F.2d 760, 218 U.S.P.Q. 781 (Fed. Cir. 1983). In this case, each and every feature of the presently claimed invention is not identically shown in the cited reference, arranged as they are in the claims.

Applicants first address the rejection of claim 1. Claim 1 is as follows:

> 1. (Previously Presented) A method of processing errors in a computer system, having at least one processor, memory, and a bus coupled between the memory and the processor, comprising:
> identifying, by a service processor, failed hardware of the computer system;
> identifying, by the service processor, other hardware affected by the failed hardware within the computer system;
> deconfiguring the failed hardware and the other hardware affected by the failed hardware; and
> rebooting the computer system without running a diagnostic on the failed hardware.

Ademmer fails to anticipate claim 1 because *Ademmer* does not teach each and every element recited in claim 1. Specifically, *Ademmer* does not teach "identifying, by a service processor, failed hardware of the computer system." The Examiner states "*Ademmer* discloses that the system controller can identify a failure (Lines 13-15 of Column 1)." Final office action of March 6, 2007, p. 2. However, the Examiner misinterpreted this portion of *Ademmer*. The cited portion of *Ademmer* is as follows:

> In the services sectors, data processing devices are increasingly being used in order to be able to serve customers even at times when there is little traffic, without people being employed for this purpose. Since the devices are only seldom used, it is desirable to disconnect the devices until a customer would like to carry out an operation.
>
> *However, this persistently fails because the initialization phase of a computer-controlled device can last for several minutes and the customer should not be expected to wait for this period of time.*

Ademmer, col. 1, lines 8-15 (Examiner's cited portion in italics).

The above portion of *Ademmer* states that disconnecting devices that are seldom used until a customer wants to carry out an operation would be desirable. However, *Ademmer* states that this idea fails because this technique would take too long to initiate the disconnected device, and because the customer should not be expected to wait. This portion of *Ademmer* and the remaining portions of *Ademmer* clearly do not teach "identifying, by a service processor, failed hardware of the computer system" as recited in claim 1.

Additionally, *Ademmer* does not teach "identifying, by the service processor, other hardware affected by the failed hardware within the computer system." The Examiner states "*Ademmer* discloses a system wherein the device controller can identify hardware as having a failure via a POST test (Lines 37-39 of Column 2)." Final office action of March 6, 2007, p. 2. The portion of *Ademmer* cited by the examiner is as follows:

> In the normal case, however, the order is accepted and is recorded in the nonvolatile memory 3. Step 13 is a waiting loop in which either there is a wait for disconnection by the device 2 via the link 7 or this command is effected via the link 6 itself. The device is then in a switched-off state, indicated by the dotted arrow. Device 2 remains operationally available and recognizes that the device 1 might be required from an external event, for example a light barrier (not shown) which indicates the approach of a potential user, or an input on a keyboard (not shown). The device 2 therefore switches the device 1 on via the link 7, at step 15. Immediately after being switched on, the device 1 begins a test routine which is always run through upon activation and tests the basic functions and extracts operating parameters from the nonvolatile memory 3. This operation is also referred to as POST, "Power On Self Test". In step 16, it is determined whether the data in the nonvolatile memory 3 contain a flag indicating that temporary disconnection occurred. *If this flag is present, then those parts of the POST which are designated symbolically by step 17 are not executed. These include comprehensive tests of the functions of the device 1 which have proven to be useful particularly after a relatively long operating intermission.* These include, for example, memory tests with different patterns in order to discover instances of data locking. These tests are unnecessary after temporary disconnection. Furthermore, these tests may be ones which test the interaction of a plurality of components. Such a test is practical particularly when components have been replaced due to repair. Furthermore, an extensive test of the consistency of the parameters stored in the nonvolatile memory, in particular of whether there is

> agreement with the installed components, can be omitted after a temporary disconnection.

Ademmer, col. 2, ll. 19-52 (emphasis to show portions cited by the examiner).

Even if *Ademmer* identified failed hardware, which Applicants have shown that Ademmer does not, neither this portion nor any portion of *Ademmer* teaches identifying hardware *affected by* the failed hardware within the computer system. Instead, the cited portion of *Ademmer* teaches that after being switched on, a device performs a power-on self test. If data in non-volatile memory contains a flag that indicates that a temporary disconnection occurred, then those parts of the POST which are designated symbolically are not executed. The "parts" are comprehensive tests of the functions of a device which have been proven to be useful particularly after a relatively long operating intermission. Examples include memory tests.

However, these functions are not related to identifying hardware *affected by* the failed hardware, as in claim 1. Manifestly, on the face of the disclosure in *Ademmer*, these functions have nothing to do with *identifying* hardware *affected by* the failed hardware, as claimed. At best, the flag in *Ademmer* indicates which functions that should not be executed. The flag does not identify hardware *affected by* the failed hardware. Nothing else in *Ademmer* teaches this claimed feature.

Furthermore, *Ademmer* does not teach "deconfiguring the *failed* hardware and the other hardware affected by the failed hardware," as recited in claim 1. The presently claimed invention clearly states deconfiguring hardware that has failed. The Examiner states *Ademmer* discloses a system that can deactivate a hardware component and save the information of configuration on CMOS-ROM. However, *Ademmer* does not deconfigure *failed* hardware. *Ademmer* temporarily disconnects working devices for the purpose of saving power (*Ademmer*, col. 1, lines 5-6). *Ademmer* states, "Before the respective device is disconnected, it is informed that the disconnection is for the purpose of saving energy." (*Ademmer*, col. 1, 45-47). Thus, *Ademmer*'s device has not failed prior to disconnection. Moreover, *Ademmer* teaches that the disconnected device can be reactivated when needed, further proving that the device has not failed. Therefore, *Ademmer* does not teach "deconfiguring the *failed* hardware and the other hardware affected by the failed hardware" as recited in claim 1.

Lastly, *Ademmer* does not teach "*rebooting the computer system* without running a diagnostic on the failed hardware," as recited in claim 1. The Examiner states *Ademmer* discloses a system that can deactivate a hardware component and upon activation, does not test or diagnose the hardware. Assuming, *arguendo*, that the examiner's statement is correct, *Ademmer* does not teach this claimed feature. Instead, *Ademmer* reactivates the previously disconnected device without executing tests and diagnostic routines on the device, however, *Ademmer* does not teach the computer system being rebooted, as claimed.

As shown above, *Ademmer* does not teach all of the features of claim 1. Therefore, under the standards of *In re Bond*, *Ademmer* does not anticipate claim 1. The remaining claims all contain features similar to those presented in claim 1. Therefore, at least for the reasons presented above, *Ademmer* does not anticipate any of the claims. Furthermore, the dependent claims also contain features not shown in *Ademmer*. Accordingly, the rejection of claims 1, 2, and 4-20 has been overcome.

II. Conclusion

The subject application is patentable over *Ademmer* and should now be in condition for allowance. The Examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the Examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

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Respectfully submitted,

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